VLSI-SoC 2024: Industrial Papers

October 6-9, 2024
Tanger, Morocco
https://vlsisoc2024.nl/



Call for Industrial paper: VLSI-SOC 2024 will host a paper presentation track dedicated industrial and to contributions. Works applicable to this track are all referring to report novel industry practices in test and new ideas in early stage of development where preliminary results are available. Moreover, all papers with at least one contributor from the industry, submitted for inclusion in the main programs but not accepted will be eligible for inclusion in the industrial track. You are invited to participate and submit your contributions to the industrial track of VLSI-SoC'24.

Guideline: Each submitted paper should be a complete PDF manuscript, from two (2) pages (extended abstract) up to 6 pages including all figures, tables, and bibliography in a standard IEEE format: A4 pages, two columns, single spaced, 10 points Times New Roman font.

Publication: All accepted industrial papers will be published in the Informal Digest of Papers upon acceptance. A page limit of 6 pages is applicable here. The papers will be labeled with "Industrial Paper".

Contact Information: For more information, please contact the Industrial Track Chair:

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VLSI-SoC 2024 is the 32th in a series of international conferences sponsored by IFIP WG 10.5, IEEE CEDA, and IEEE CASS, which explore the state-of-the-art in the areas of Very Large Scale Integration (VLSI) and System-on-Chip (SoC) design. The purpose of VLSI-SoC is to provide a forum to exchange ideas and showcase academic as well as industrial research in architectures, circuits, devices, design automation, verification, test, and security, within digital, analog, and mixed-signal systems. VLSI-SoC'24 will take place at hotel Barcelo, Tanger, Morocco, and it is organized by the Delft University of Technology.

VLSI-SoC 2024 will be held under the theme "SoCs for 5G Evolution and 6G" exploring the design and optimization challenges around 5G+6G communication systems and devices embedded systems, security, low power circuits, powered by CMOS and beyond CMOStechnologies.



The areas of interest include (but are not limited to) the following topics:

- Analog, mixed-signal, RF, and sensors
- Digital circuits, low-power design, SoC, NoC, and reconfigurable architectures
- Design for AI acceleration and machine learning for SoC design
- · Circuits and systems for signal processing and communications
- · Modelling, simulation, verification, and prototyping
- · EDA tools and methodologies for IC design
- Design for testability, reliability, and fault tolerance
- Hardware security
- IoT, embedded and cyber-physical systems: Architecture, design, and Software
- Emerging computing paradigms: Quantum computing, cryogenic processors
- 5G / 6G emerging technologies

General Chairs: Said Hamdioui, Delft University of Technology (NL) & Anass El Haddadi, ENSA (MA)

Program Chairs: Hussam Amrouch, Technical University of Munich (DE) & Ioana Vatejelu, TIMA Grenoble (FR)

Tutorial Chair: Leticia M.B. Pöhls. RWTH Aachen University (DE)

Special Session Chairs: Baker Mohammad, Khalifa University (AE) & Saraju Mohanty, University of North Texas (US)

Panel Chairs: Hassen Aziza, Aix-Marseille Université & Annachiara Ruospo, Politecnico di Torino (IT)

Awards Chairs: Fatih Ugurdag, Özyeğin University (TR) & Tiziana Margaria, University of Limerick (IE)

PHD Forum Chair: Florenc Demrozi, University of Stavanger (NO)

Publication Chairs: Moritz Fieback, Delft University of Technology (NL) & Anteneh Gebregiorgis, Delft University of Technology (NL)

Finance Chairs: Motta Taouil, Delft University of Technology (NL) & Carlo Galuzzi, Delft University of Technology (NL)

Web Chair: Heba Abunahla, Delft University of Technology (NL) & Mark van Beusekom, Delft University of Technology (NL)

Sponsoring Chairs: Mohamed Bouhorma, Abdelmalek Essaâdi University (AE) Local Arrangement Chairs: Nabila Harboul, Future Professionals Academy (NL) & Jaber El Bouhdidi, ENSA (MA)







