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جامعة عبد المالك السعدي
Université Abdelmalek Essaâdi

Contents

Day 0: Sunday 06

Tutorial 1 - Part 1 09:00–10:30

Artificial intelligence: from fundamentals to Applications

Kaushik Roy

Purdue University

Artificial Intelligence (AI) is transforming industries and shaping the future of technology. This tutorial provides a comprehensive introduction to the fundamentals of AI, designed for beginners and enthusiasts seeking to understand the core concepts and applications. We will explore the history and evolution of AI, key terminologies, and foundational principles, including machine learning, regression, different flavours of neural networks, robustness and security aspects of AI, AI hardware, etc. Through practical examples and case studies, attendees will gain insights into how AI systems are developed and deployed in various fields. By the end of this tutorial, participants will have a solid grounding in AI concepts and be equipped with the knowledge to delve deeper into specialized AI domains.

Coffee Break	**10:30–11:00**
Tutorial 1 - Part 2	**11:00–12:30**
Lunch	**12:30–14:00**
Tutorial 2 - Part 1	**14:00–15:30**

Computers: from Intel 4004 to Neuro Chips

Henk Corporaal

Technical University of Eindhoven

In 1971 Intel designed the first single chip microprocessor, the 4-bit 4004 processor. Since then, the area of computer architecture has shown an unprecedented growth in performance, from roughly 10 kOps/Sec to more than 100 TOps/Sec, that's about 100x every decade, and that 5 decades! How was this possible, and will this continue? While performance is still very important, since about two decades energy efficiency took over as main driver of today's processor design. What caused this change of focus? To increase efficiency architects are often trading flexibility; is this smart? Processors are used almost everywhere, in a wide range of application domains. Therefore, we see many flavors, ranging from generic, general purpose processors, as used in PCs and laptops, to highly dedicated and specialized ones, like used in the signal processing domain. The last decade shows a new application development, the rise of deep learning, impacting all aspects of our life. The

networks for deep learning increased by 100,000x in ten years. This is even beyond the imagination of a computer architect. How can we deal with this, what is its impact on computer architecture?

Coffee Break	**15:30–16:00**
Tutorial 2 - Part 2	**16:00–17:30**
Welcome Reception	**18:30–20:30**

Day 1: Monday 07

Opening 08:30–09:00

Keynote 1 09:00–10:00

AI at the edge: Hype or Hope?

Henk Corporaal

Eindhoven University of Technology

Artificial neural networks (ANNs), especially deep ones, have gained immense popularity. While their potential applications appear boundless, a significant drawback is their heavy reliance on cloud-based servers. This dependence stems from the exponential expansion in the size and computational requirements of these networks. For instance, the latest large language models like ChatGPT-4 boast over a trillion parameters and demand astonishing computational resources, in the order of 10^{25} FLOPS, for training. Achieving this training task in a reasonable timeframe (i.e., less than a month) requires the use of thousands of cloud-based servers. Even a single inference takes about 5.10^{14} FLOPS, making real-time inferencing extremely costly. We believe that there are substantial advantages in bringing intelligence directly to smart sensor devices at the network edge, performing the computation locally, close to the sensing data. However, these devices typically have

a sub-Watt or even sub-mWatt power budget, and lack huge memories and compute capabilities. Achieving smart Edge-AI with less reliance on large AI servers necessitates a significant improvement in energy efficiency. This leads to the question: is AI at the edge really feasible, or is it a mindless dream? In this keynote, we address the state of the art (SOTA) in Edge computing and its trends and developments. We discuss what is needed to really bring AI to the Edge, how to bridge this huge energy-efficiency gap. Improvements are needed at all levels of the design stack; perhaps even new neural computing paradigms. We conclude by offering a glimpse into the future, exploring potential breakthroughs on the horizon.

Coffee Break 10:00–11:00

Regular Session 1: Security 11:00–12:30

A Novel Design Technique for Enhanced Security and New Applications of Ferroelectric-based Non-Volatile SRAM

Lucas RHETAT, Jean-Philippe NOEL, Bastien GIRAUD, Laurent GRENOUILLET, Julie LAGUERRE, Cedric MARCHAND, Ian O CONNOR

CEA, CEA, CEA, CEA, CEA, Ecole centrale of Lyon, Ecole Centrale de Lyon

Capture the Pulse: Impact of FPGA Resource Utilization on EM Fault Injection Attacks Detection

Sami EL AMRAOUI, Regis LEVEUGLE, Paolo MAISTRI

TIMA, Grenoble INP, CNRS

Continuity in Security: Leveraging LLM for Translating Security Properties Across Hardware Designs (Best paper candidate)

Bulbul AHMED, Sujan KUMAR SAHA, Jingbo ZHOU, Sohrab AFTABJA-

HANI, Mark TEHRANIPOOR, Farimah FARAHMANDI

University of Florida, University of Florida, University of Florida, Intel Corporation, University of Florida, University of Florida

OSHDA: A Containerized CAD Tool for the Design and Analysis of Behavioral FSM Logic Locking

Esrat KHAN, Shahzad MUZAFFAR, Lamees AL QASSEM, Abe ELFADEL

Khalifa University, Philips, Khalifa University, Khalifa University

Special Session 1 11:00–12:30

Reliability Assessment Of Neural Networks: Trading-Off Between Performance and Accuracy

Juan GUERRERO, Matteo SONZA REORDA, Angeliki KRITIKAKOU, Marcello TRAIOLA, Josie RODRIGUEZ CONDIA, Junchao CHEN, Milos KRSTIC, Alessandro VERONESI, Fernando DOS SANTOS, Robert LIMAS SIERRA, Giuseppe ESPOSITO

Politecnico di Torino1, Politecnico di Torino, Univ Rennes, INRIA, Irisa, INRIA, Politecnico di Torino, Innovations for High Performance Microelectronics, IHP, IHP - Microelectronics, INRIA, Politecnico di Torino, Politecnico di Torino

Lunch 12:30–14:00

Regular Session 2: Miscellaneous 14:00–16:00

APPAMM: Memory Management for IPsec Application on Heterogeneous SoCs (Best paper candidate)

Ayushi AGARWAL, Radhika DHARWADKAR, Isaar AHMAD, Krishna KUMAR, P. J. JOSEPH, Sourav ROY, Prokash GHOSH, Preeti Ranjan PANDA

IIT Delhi, IIT Delhi, NXP Semiconductors, IIT Delhi, NXP Semiconductors, NXP Semiconductors, NXP Semiconductors, NXP Semiconductor, Inc, USA, IIT Delhi

Minimum Depth Quantum Modular Addition through Carry-Save Architecture (Best paper candidate)

Siyi WANG, Eugene LIM, Xiufan LI, Jerrie FENG, Anupam CHATTOPADHYAY

Nanyang Technological University, Nanyang Technological University, National University of Singapore, Nanyang Technological University, Nanyang Technological University

NEATRouter: An New Method for 2D Global Routing

Luis MURILLO VIZCARDO, Ricardo REIS

Universidade Federal do Rio Grande do Sul, Universidade Federal do Rio Grande do Sul

Embedded and Real-Time Anomalous Command Classification in Unmannded Ground Vehicle Operations

Rafaella ELIA, Theocharis THEOCHARIDES

University of Cyprus, University of Cyprus

Low Power Network-on-Chip Architecture Design Technique

Tejas MUSALE, Arun GANTI, Ankur GOGOI, Kanchan MANNA

BITS Pilani Goa Campus, BITS Pilani Goa Campus, BITS Pilani Goa Campus, BITS Pilani Goa Campus

Industrial Session 14:00–16:00

Advanced Heterogenous System Integration: Challenges and Cadence Solution

Fadoua Gacim, Tal Zigman, Franck Gerome

Cadence, Cadence, Cadence

A Novel Approach to Perform an Automated Validation of Radar Emulation Platform Using Qualification Framework

Sooraj RAVINDRAKUMAR, Ankita GUPTA, Jayakrishna GUDDETI

Infineon Technologies, Infineon Technlogies India Pvt Ltd, Infineon Technologies

A Unified Functional Safety EDA Framework for Accurate Diagnostic Coverage Estimation

Abhiroop BHOWMIK , Subin BABUKUTTY , Mottaqiallah TAOUIL, Moritz FIEBACK

Delft University of Technology, NXP, Delft University of Technology, Delft University of Technology

Coffee Break 16:00–16:30

PhD Forum 16:30–18:00

Panel 1 18:00–19:30

Day 2: Monday 08

Keynote 2 09:00–10:00

Long Live Computing Technology

Rajiv Joshi

IBM

The explosion of computers and the internet significantly improved the quality of human life. Communication across the globe made the earth as one family. Building blocks of this computing power are fabricated from crucial and key semiconductor technology. This talk covers such building blocks and showcases their impact. Volatile and non-volatile memories (NVM) have proved to be focal points for research over decades. Memories in general are the workhorse of the semiconductor industry. Applications of these spread across many domains such as Artificial Intelligence (AI), servers, high-performance computing, Systems on Chip (SOC), Internet of Things (IoT), quantum computing, etc., and thus are essential components of the computing world. As we march forward the scaling of memories poses a major challenge to achieve functionality, performance, area, power, and yield. To overcome scaling issues the talk will describe alternative techniques and circuits. It will bring out challenges and future directions for various memory applications.

Poster Session 1 & Coffee Break

10:00–11:00

3D VNWFET-Based Standard Cell Library Design Flow: From Circuit and Physical Design to Logic Synthesis

Sara MANNAA, Ian O CONNOR, ALBERTO BOSIO, Bastien DEVEAUTOUR, Cedric MARCHAND, Damien DELERUYELLE, Osakr BAUMGARTNER, Christoph LENZ

Ecole Centrale de Lyon, Ecole Centrale de Lyon, Lyon Institute of Nanotechnology, CPE Lyon, Ecole Centrale de Lyon, INL, , Global TCAD Solutions GmbH (GTS)

A New Control Law for N-Path Mixer Switches Enhancing Harmonic Rejection

Hasan MOUSSA, Estelle LAUGA-LARROZE, Laurent FESQUET

TIMA, TIMA, TIMA laboratory

A Scalable Hardware Architecture for Efficient Sequential Learning at the Edge

Yicheng ZHANG, Manil Dev GOMONY, Corporaal HENK, Federico CORRADI

Eindhoven University of Technology, Electronic Systems Group, Eindhoven University of Technology, Eindhoven University of Technology

An Efficient Performance-driven Analog IC Placement Optimizer via Extremely Randomized Tree-based Post-Layout Performance Regressors

Ricardo MARTINS, Nuno LOURENCO

Instituto de Telecomunicações / Instituto Superior Técnico - University of Lisbon, IT

ASIP Acceleration for SNN Computation Based on RISC-V

Liangshun WU, Jianwei XUE, Peilin LIU

Shanghai Jiao Tong University, School of Electronic and Electrical Engi-

neering, Shanghai Jiao Tong University, School of Electronic and Electrical Engineering, Shanghai Jiao Tong University

Commercial Evaluation of Zero-Skipping MAC Design for Bit Sparsity Exploitation in DL Inference

Harideep NAIR, Prabhu VELLAISAMY, Tsung-Han LIN, Perry WANG, Shawn BLANTON, John SHEN

Carnegie Mellon University, Carnegie Mellon University, Mediatek, Mediatek, Carnegie Mellon University, Carnegie Mellon University

Compensating of the Load Effect in Quadrature All-Pass Filters

Uxua ESTEBAN ERASO, Carlos SáNCHEZ-AZQUETA, Francisco AZNAR, Concepción ALDEA, Santiago CELMA

Universidad de Zaragoza, Universidad de Zaragoza, Universidad de Zaragoza, Universidad de Zaragoza, Universidad de Zaragoza

Design Co-Processor based on Partially Homomorphic Encryption Execution Using OpenSource Tool

Muhammad BHATTI, Mujahid BILAL

National Institute of Electronics, National Institute of Electronics

Enhancing Security Against Reverse-Engineering Attacks Using Structure Rephrasing

Kaixin YANG, Subhajit DUTTA CHOWDHURY, Pierluigi NUZZO

University of Southern California, University of Southern California, University of Southern California

Exploiting Functional Approximation on Decision-Tree based Multiple Classifier Systems

Antonio EMMANUELE, Mario BARBARESCHI, Salvatore BARONE, Nicola MAZZOCCA

Università Federico II di Napoli, University of Naples Federico II, University of Naples Federico II, University of Naples Federico II

FortRoot: Fortifying Rooted-in-Device-Specific Security through Secure Booting

Sajeed MOHAMMAD, Farimah FARAHMANDI

University of Florida, University of Florida

FVDCLS: Functional Verification of RISCV based Dual-Core Lock-step Feature using Fault Injection Mechanism

Muhammad MINHAS, Haroon WARIS, Sajid BALOCH

CESTA, Nanjing University of Aeronautics and Astronautics (NUAA), CESTA

Heterogeneous Approximation of DNN HW Accelerators based on Channels Vulnerability

Natalia CHEREZOVA, Salvatore PAPPALARDO, Mahdi TAHERI, Mohammad Hasan AHMADILIVANI, Bastien DEVEAUTOUR, ALBERTO BOSIO, Jaan RAIK, Maksim JENIHHIN

Tallinn University of Technology, Ecole Centrale de Lyon, Tallinn University of Technology, , CPE Lyon, Lyon Institute of Nanotechnology, Tallinn University of Technology, Tallinn University of Technology

Regular Session 3: Simulation, Verification and Safety 11:00–12:30

Linear Algebra Approach to Verification of Modular Multipliers

Jiteshri DASARI, Cunxi YU, Maciej CIESIELSKI

University of Massachusetts Amherst, University of Maryland, College Park, University of Massachusetts Amherst

Behavioral Simulation of Relative Timed Asynchronous circuits

Sumanth KOLLURU, Kenneth S. STEVENS

University of Utah, University of Utah

Adaptable FWHW Formal Co-Verification of SoC RISC-V Compo-

nents

Paulette ISKANDAR, Bryan OLMOS, Wolfgang KUNZ, Djones LETTNIN

Infineon Technologies AG, Infineon Technologies AG, Rheinland-Pfälzische Technische Universität Kaiserslautern-Landau, Infineon Technologies AG

Diagnostic Coverage Estimation for Automotive SoCs based on Colored Stochastic Petri Nets

Ernesto Cristopher VILLEGAS CASTILLO, Felipe AUGUSTO DA SILVA, Michael GLASS

Cadence Design Systems, Cadence Design Systems, Institute of Embedded Systems/Real-Time Systems, Ulm University

Regular Session 4: Design for AI
11:00–12:30

Adaptive block-scaled GeMMs on vector processors for DNN training at the edge (Best paper candidate)

Nitish SATYA MURTHY, Nathan LAUBEUF, Debjyoti BHATTACHARJEE, Francky CATTHOOR, Marian VERHELST

KU Leuven - IMEC, IMEC, IMEC, IMEC Belgium, KU Leuven - IMEC

Stochastic Spintronics Device Based Bayesian Networks for Efficient Uncertainty Modeling

ALISHA PB, Tripti WARRIER

Cochin University of Science and Technology, Cochin University of Science and Technology

A High Throughput, Energy-Efficient Architecture for Variable Precision Computing in DRAM

Gian SINGH, Ayushi DUBE, Sarma VRUDHULA

Arizona State University, , Arizona State University

GemIMC: A Configurable HW Architecture for Technology Agnostic IMC based NN Inference

Emilien TALY, Roberto GUIZETTI, Pascal URARD, Elena Ioana VATAJELU

TIMA Laboratory and ST Microelectronics, STMicroelectronics, STMicroelectronics, TIMA Laboratory

Lunch 12:30–14:00

Embedded Tutorial 1 14:00–15:00

New Computing Paradigm For Large Language Models (LLMs)

Sumit MANDAL

Indian Institute of Science

Embedded Tutorial 2 14:00–15:00

On-Chip Infrastructure For MissionMode Monitoring Of Resilient Systems: Towards Silicon Lifecycle Management

Fabian VARGAS

IHP - Microelectronics

Social Event 15:00–20:30

Day 3: Wednesday 09

Keynote 3 09:00–10:00

Secure Heterogeneous Integration and Advanced Packaging: New Attack Surfaces and Grand Challenges Ahead

Mark M. Tehranipoor

University of Florida (US)

Heterogeneous integration and advanced packaging have seen resurgence over the past few years. The notion of building a system in package from chiplets is quite attractive, however it comes with challenges of ensuring quality, reliability and security. Providing assurance for each chiplet, establishing a secure chiplet supply chain, ensuring secure and trusted integration, verifying and validating policies, etc are few important challenges that will be discussed in this presentation.

Poster Session 2 & Coffee Break 10:00–11:00

High-Density Standard Cell Library for Sequential 3D Integrated Circuits

Arturo PRIETO, Joachim RODRIGUES

Lund University, Lunds University

Holistic Framework for Evaluating the Trustworthiness of Integrated Circuits

Mouadh AYACHE, Enkele RAMA, Saleh MULHEM, Mladen BEREKOVIC, Matthias KORB

Synopsys GmbH Munich, Universität der Bundeswehr München, Institute of Computer Engineering Universität zu Lübeck , University of Luebeck, Institut for Integrated Systems Universität der Bundeswehr München

Lightweight Active Fences for FPGAs

Anis FELLAH-TOUTA, Lilian BOSSUET, Carlos Andres LARA-NINO, Vincent GROSSO

CNRS, University St Etienne, University Rovira i Virgili, Laboratoire Hubert Curien

MCS-NTT: Multi-Chip System Design for NTT Acceleration

Mohammed Nabeel MOOPAN, Homer GAMIL, Johann KNECHTEL, Maniatakos MIHALIS

New York University Abu Dhabi, New York University, New York University Abu Dhabi, NYU Abu Dhabi

MEAN: Mixture-of-Experts Based Neural Receiver

Bram BOLDERIK, Vlado MENKOVSKI, Sonia HEEMSTRA, Manil Dev GOMONY

Technical university of eindhoven, Technical university of eindhoven, Technical university of eindhoven, Electronic Systems Group

Resistance switching properties of stoichiometric and nitrogen implanted silicon nitride structures on heavily doped Si substrates

Alexandros MAVROPOULIS, Panagiotis KARAKOLIS, Nikolaos VASILEIADIS, Labrini SYGELLOU, Emmanouil STAVROULAKIS, Vassilios IOANNOUSOUGLERIDIS, Pascal NORMAND, Georgios Ch. SIRAKOULIS, Panagiotis DIMITRAKIS

NCSR Demokritos, NCSR Demokritos, NCSR Demokritos, Institute of

Regular Session 5: Memories 11:00–12:30

FeFET-based CAM Address Decoders

Thomas MAKRYNIOTIS, Georgi GAYDADJIEV, Said HAMDIOUI, Mottaqiallah TAOUIL

Delft University of Technology, Delft University of Technology, Delft University of Technology, Delft University of Technology

In-Memory Mirroring: Cloning Without Reading

Simranjeet SINGH, Ankit BENDE, Chandan KUMAR JHA, Vikas RANA, Rolf DRECHSLER, Sachin PATKAR, Farhad MERCHANT

IIT Bombay, Forschungszentrum Jülich, University of Bremen, Forschungszentrum Jülich, Uni. Bremen, IIT Bombay, Newcastle University

AFSRAM-CIM: Adder Free SRAM-Based Digital Computation-in-Memory for BNN

Asmae EL ARRASSI, Mohammad Amin YALDAGARD, Xingjian TAO, Taha SHAHROODI, Fouwad MIR, Yashvardhan BIYANI, Manil Dev GOMONY, Anteneh GEBREGIORGIS, Rajiv JOSHI, Said HAMDIOUI

Delft University of Technology, Technische Universiteit Delft, Eindhoven University of Technology, Delft University of Technology, Delft University of Technology, Delft University of Technology, Electronic Systems Group, Delft University of Technology, IBM T.J., Watson, USA, Delft University of Technology

DynaCache: A checkpoint aware reconfigurable cache for Intermittently powered computing systems

Rishabh MAHANTA, Hemangee KAPOOR

Indian Institute of Technology Guwahati, Indian Institute of Technology Guwahati

Special Session 2 11:00–12:30

IoT-Enabled Electronics For Smart Agriculture

Laavanya RACHAKONDA, Alakananda MITRA, Saraju MOHANTY

University of North Carolina at Wilmington, University of Nebraska-Lincol, University of North Texas

Lunch 12:30–14:00

Regular Session 6: Analog, Microfluidics, Aging 14:00–15:30

A Low-Power Linear Phase Interpolation-Based Delay Line in 12nm FinFET Technology

Mohammadreza ESMAEILPOUR, Jan LAPPAS, Christian WEIS, Norbert WEHN

University of Kaiserslautern-Landau, University of Kaiserslautern-Landau, RPTU Kaiserslautern-Landau, RPTU Kaiserslautern-Landau

Design of a very Low Noise Figure Wideband LNA with Differential Output for RF reciever applications

Rohit KUMAR, Heena MULLA, S NAGAVENI

Indian Institute of Technology, Indian Institute of Technology Dharwad, Indian Institute of Technology Dharwad

Benchmarking Microfluidic Design Automation Flows

Ashton SNELGROVE, Skylar STOCKHAM, Pierre-Emmanuel GAILLARDON

University of Utah, University of Utah, University of Utah

Understanding Transistor Aging Impact on the Behavior of RRAM Cells

Seyed Hossein HASHEMI SHADMEHRI, Supriya CHAKRABORTY, Thiago COPETTI, Fabian VARGAS, Leticia BOLZANI POEHLS

RWTH Aachen University, RWTH Aachen University, RWTH Aachen University, IHP - Microelectronics, RWTH Aachen University

Special Session 3 14:00–15:30

Embedded Hardware Security: Primitives, Architectures, and Test

Farhad MERCHANT, Saleh MULHEM

Newcastle University, Institute of Computer Engineering, Universität zu Lübeck

Coffee Break 15:30–16:00

Panel 2 16:00–17:30

Special Session 4 16:00–17:30

Security by Design

Venkata Prasanth YANAMBAKA, Robert KARAM, Saraju MOHANTY

Texas Woman's University, University of South Florida, University of North Texas

Closing 17:30–18:00